We claim:

1. A method of data transmission comprising the steps of:

transmitting transmit data over a first set of time slots, wherein the transmit data includes in-phase transmit data bits and quadrature phase transmit bits; and

transmitting various uplink low rate static/control signals over a second set of time slots.

2. The method of claim 1, wherein the in-phase transmit data bits comprises of a first in-phase transmit data bit and a second in-phase transmit data bit, the first in-phase transmit data bit being transmitted over a first time slot in the first set of time slots and the second in-phase transmit data bit being transmitted over a second time slot in the first set of time slots.

3. The method of claim 2, wherein the quadrature phase transmit data bits comprises of a first quadrature phase transmit data bit and a second quadrature phase transmit data bit, the first quadrature phase transmit data bit being transmitted over a third time slot in the first set of time slots and the second quadrature phase transmit data bit being transmitted over a fourth time slot in the first set of time slots.

4. The method of claim 1, wherein the various uplink low rate static/control signals include one or more of the following: clock/reference signals, uplink RS-485 based bus data, physical address information, adjacent CDMA channel unit availability information, input information via uplink serial ports and a radio RF emergency switch.

5. The method of claim 4, wherein two or more of the various uplink low rate static/control signals are multiplexed for transmission over a first time slot in the second set of time slots.

6. The method of claim 4, wherein the uplink RS-485 based bus data includes two bits and is transmitted over a first and second time slot in the second set of time slots.

7. The method of claim 6, wherein the clock/reference signals, adjacent CDMA channel unit availability information, input information via uplink serial ports and a radio RF emergency switch are multiplexed for transmission over a third time slot in the second set of time slots.

8. The method of claim 7, wherein the physical address information is multiplexed for transmission over a fourth time slot in the second set of time slots.

9. The method of claim 1 comprising the additional step of:

transmitting a multiplex synchronization pulse over a first time slot in a third set of time slots.

10. The method of claim 9 comprising the additional step of:

transmitting a parity bit over a second time slot in the third set of time slots.

11. The method of claim 1 comprising the additional step of:

transmitting coding bits over a plurality of time slots in a third set of time slots.

12. The method of claim 1 comprising the additional step of:

receiving a downlink serial data stream comprising of receive data over a third set of time slots and various downlink low rate static/control signals over a fourth set of time slots.

13. The method of claim 12, wherein the receive data includes two bits of in-phase receive data bits received over a first antenna, two bits of in-phase receive data bits received over a second antenna, two bits of quadrature phase receive data bits received over the first antenna, two bits of quadrature phase receive data bits received over the second antenna.

14. The method of claim 13, wherein the two bits of in-phase receive data bits received over the first antenna were received over a first and second time slot in the third set of time slots, two bits of in-phase receive data bits received over the second antenna were received over a third and fourth time slot in the third set of time slots, two bits of quadrature phase receive data bits received over the first antenna were received over a fifth and sixth time slot in the third set of time slots, two bits of quadrature phase receive data bits received over the second antenna were received over a seventh and eighth time slot in the third set of time slots.

15. The method of claim 12, wherein the various downlink low rate static/control signals include one or more of the following: bypass information, input information via downlink serial ports and downlink RS-485 based bus data.

16. The method of claim 15, wherein two or more of the various downlink low rate static/control signals are multiplexed for transmission over a first time slot in the fourth set of time slots.

17. The method of claim 16, wherein the bypass information and input information via downlink serial ports are multiplexed for transmission over the first time slot in the fourth set of time slots.

18. The method of claim 16, wherein the downlink RS-485 based bus data is transmitted over a second time slot in the fourth set of time slots.

19. The method of claim 12 comprising the additional step of:

transmitting a multiplex synchronization pulse over a first time slot in a fifth set of time slots.

20. The method of claim 19 comprising the additional step of:

transmitting a parity bit over a second time slot in the fifth set of time slots.

21. The method of claim 12 comprising the additional step of:

transmitting coding bits over a plurality of time slots in a fourth set of time slots.

22. A method of data transmission comprising the steps of:

transmitting receive data over a first set of time slots, wherein the receive data includes in-phase transmit data bits and quadrature phase transmit bits; and

transmitting various downlink low rate static/control signals over a second set of time slots.

23. The method of claim 22, wherein the receive data includes two bits of in-phase receive data bits received over a first antenna, two bits of in-phase receive data bits received over a second antenna, two bits of quadrature phase receive data bits received over the first antenna, two bits of quadrature phase receive data bits received over the second antenna.

24. The method of claim 23, wherein the two bits of in-phase receive data bits received over the first antenna are transmitted over a first and second time slot in the first set of time slots, two bits of in-phase receive data bits received over the second antenna are transmitted over a third and fourth time slot in the third set of time slots, two bits of quadrature phase receive data bits received over the first antenna are transmitted over a fifth and sixth time slot in the third set of time slots, two bits of quadrature phase receive data bits received over the second antenna are transmitted over a seventh and eighth time slot in the third set of time slots.

25. The method of claim 22, wherein the various downlink low rate static/control signals include one or more of the following: bypass information, input information via downlink serial ports and downlink RS-485 based bus data.

26. The method of claim 25, wherein two or more of the various downlink low rate static/control signals are multiplexed for transmission over a first time slot in the second set of time slots.

27. The method of claim 26, wherein the bypass information and input information via downlink serial ports are multiplexed for transmission over the first time slot in the second set of time slots.

28. The method of claim 26, wherein the downlink RS-485 based bus data is transmitted over a second time slot in the second set of time slots.

29. The method of claim 22 comprising the additional step of:

transmitting a demultiplex synchronization pulse over a first time slot in a third set of time slots.

30. The method of claim 29 comprising the additional step of:

transmitting a parity bit over a second time slot in the third set of time slots.

31. The method of claim 22 comprising the additional step of:

transmitting coding bits over a plurality of time slots in a third set of time slots.

32. An interface for data transmission comprising of:

a first set of parallel transmission mediums;

a complex programmable logic device connected to a plurality of digital components and connected to one end of the first set of parallel transmission mediums, the complex programmable logic device being operable to accept transmit data and various uplink low rate static/control data from the plurality of digital components, to multiplex the transmit data or various uplink low rate static/control data, and to send the transmit data and various uplink low rate static/control data over the first set of parallel transmission mediums;

a first serial transmission medium;

a serializer connected to another end of the first set of parallel transmission mediums and to one end of the first serial transmission medium, the serializer being operable to accept the transmit data and various uplink low rate static/control signals sent by the complex programmable logic device and to sequentially send the transmit data and various uplink low rate static/control signals serially over the first serial transmission medium; and

a transmitter connected to another end of the first serial transmission medium, the transmitter being operable to accept the transmit data and various uplink low rate static/control signals sent by the serializer and to send the transmit data and various uplink low rate static/control signals over another transmission medium.

33. The interface of claim 32, wherein the transmit data comprises of a first in-phase transmit data bit, a second in-phase transmit data bit, a first quadrature phase transmit data bit and a second quadrature phase transmit data bit, the complex programmable logic device being operable to transmit the first in-phase transmit data bit over a first transmission medium in the first set of parallel transmission mediums, the second in-phase transmit data bit over a second transmission medium in the first set of parallel transmission mediums, the first quadrature phase transmit data bit over a third transmission medium in the first set of parallel transmission mediums and the second quadrature phase transmit data bit over a fourth transmission medium in the first set of parallel transmission mediums.

34. The interface of claim 33, wherein the various uplink low rate static/control signals comprises of clock/reference signals, uplink RS-485 based bus data, physical address information, adjacent CDMA channel unit availability information, input information via uplink serial ports and a radio RF emergency switch, the complex programmable logic device being operable to multiplex the clock/reference signals, adjacent CDMA channel unit availability information, input information via uplink serial ports and a radio RF emergency switch to produce an uplink multiplexed data stream, the complex programmable logic device being operable to transmit the uplink multiplexed data stream over a fifth transmission medium in the first set of parallel transmission mediums, the uplink RS-485 based bus data over a sixth and seventh transmission medium in the first set of parallel transmission mediums and the physical address information over a eighth transmission medium in the first set of parallel transmission mediums.

35. The interface of claim 34 further comprising:

a second serial transmission medium;

a receiver connected to the second serial transmission medium, the receiver being operable to accept receive data and various downlink low rate static/control signals and to send the receive data and various downlink low rate static/control signals over the second serial transmission medium;

a second set of parallel transmission mediums connected at one end to the complex programmable logic device;

a deserializer connected to another end of the second set of parallel transmission mediums and to another end of the second serial transmission medium, the deserializer being operable to accept the receive data and various downlink low rate static/control signals sent by the receiver and to sequentially send the receive data and various downlink low rate static/control signals over the second set of parallel transmission mediums, the complex programmable logic device being operable to accept the receive data and various downlink low rate static/control signals sent by the deserializer and to send the receive data and various downlink low rate static/control signals to the plurality of digital components.

36. The interface of claim 35, wherein the receive data comprises of a first in-phase receive data bit, a second in-phase receive data bit, a third in-phase receive data bit, a fourth in-phase receive data bit, a first quadrature phase receive data bit, a second quadrature phase receive data bit, a third quadrature phase receive data bit and a fourth quadrature phase receive data bit, the first and second in-phase and quadrature phase receive data bits being received over a first antenna, the third and fourth in-phase and quadrature phase receive data bits being received over a second antenna, the complex programmable logic device being operable to transmit the first in-phase receive data bit over a first transmission medium in the second set of parallel transmission mediums, the second in-phase receive data bit over a second transmission medium in the second set of parallel

transmission mediums, the third in-phase receive data bit over a third transmission medium in the second set of parallel transmission mediums, the fourth in-phase receive data bit over a fourth transmission medium in the second set of parallel transmission mediums, the first quadrature phase receive data bit over a fifth transmission medium in the second set of parallel transmission mediums, the second quadrature phase receive data bit over a sixth transmission medium in the second set of parallel transmission mediums, the third quadrature phase receive data bit over a seventh transmission medium in the second set of parallel transmission mediums, the fourth quadrature phase receive data bit over a eighth transmission medium in the second set of parallel transmission mediums.

37. The interface of claim 36, wherein the various downlink low rate static/control signals comprises bypass information, input information via downlink serial ports and downlink RS-485 based bus data, the complex programmable logic device being operable to multiplex the bypass information and input information via downlink serial ports to produce a downlink multiplexed data stream, the complex programmable logic device being operable to transmit the downlink multiplexed data stream over a ninth transmission medium in the second set of parallel transmission mediums and the downlink RS-485 based bus data over a tenth transmission medium in the second set of parallel transmission mediums.

38. An interface for data transmission comprising of:

a first set of parallel transmission mediums;

a complex programmable logic device connected to a plurality of RF components and connected to one end of the first set of parallel transmission mediums, the complex programmable logic device being operable to accept receive data and various downlink

low rate static/control data from the plurality of RF components, to multiplex the transmit data or various downlink low rate static/control data, and to send the receive data and various downlink low rate static/control data over the first set of parallel transmission mediums;

a first serial transmission medium;

a serializer connected to another end of the first set of parallel transmission mediums and to one end of the first serial transmission medium, the serializer being operable to accept the receive data and various downlink low rate static/control signals sent by the complex programmable logic device and to sequentially send the receive data and various downlink low rate static/control signals serially over the first serial transmission medium; and

a transmitter connected to another end of the first serial transmission medium, the transmitter being operable to accept the receive data and various downlink low rate static/control signals sent by the serializer and to send the receive data and various downlink low rate static/control signals over another transmission medium.

39. The interface of claim 38, wherein the receive data comprises of a first in-phase receive data bit, a second in-phase receive data bit, a third in-phase receive data bit, a fourth in-phase receive data bit, a first quadrature phase receive data bit, a second quadrature phase receive data bit, a third quadrature phase receive data bit and a fourth quadrature phase receive data bit, the first and second in-phase and quadrature phase receive data bits being received over a first antenna, the third and fourth in-phase and quadrature phase receive data bits being received over a second antenna, the complex programmable logic device being operable to transmit the first in-phase receive data bit over a first transmission medium in the first set of parallel transmission mediums, the second in-phase receive data bit over a second transmission medium in the first set of parallel

transmission mediums, the third in-phase receive data bit over a third transmission medium in the first set of parallel transmission mediums, the fourth in-phase receive data bit over a fourth transmission medium in the first set of parallel transmission mediums, the first quadrature phase receive data bit over a fifth transmission medium in the first set of parallel transmission mediums, the second quadrature phase receive data bit over a sixth transmission medium in the first set of parallel transmission mediums, the third quadrature phase receive data bit over a seventh transmission medium in the first set of parallel transmission mediums, the fourth quadrature phase receive data bit over a eighth transmission medium in the first set of parallel transmission mediums.

40. The interface of claim 39, wherein the various downlink low rate static/control signals comprises bypass information, input information via downlink serial ports and downlink RS-485 based bus data, the complex programmable logic device being operable to multiplex the bypass information and input information via downlink serial ports to produce a downlink multiplexed data stream, the complex programmable logic device being operable to transmit the downlink multiplexed data stream over a ninth transmission medium in the second set of parallel transmission mediums and the downlink RS-485 based bus data over a tenth transmission medium in the second set of parallel transmission mediums.

41. The interface of claim 38 further comprising:

a second serial transmission medium;

a receiver connected to the second serial transmission medium, the receiver being operable to accept transmit data and various uplink low rate static/control signals and to send the transmit data and various uplink low rate static/control signals over the second serial transmission medium;

a second set of parallel transmission mediums connected at one end to the complex programmable logic device;

a deserializer connected to another end of the second set of parallel transmission mediums and to another end of the second serial transmission medium, the deserializer being operable to accept the transmit data and various uplink low rate static/control signals sent by the receiver and to sequentially send the transmit data and various uplink low rate static/control signals over the second set of parallel transmission mediums, the complex programmable logic device being operable to accept the transmit data and various uplink low rate static/control signals sent by the deserializer and to send the transmit data and various uplink low rate static/control signals to the plurality of RF components.

42. The interface of claim 41, wherein the transmit data comprises of a first in-phase transmit data bit, a second in-phase transmit data bit, a first quadrature phase transmit data bit and a second quadrature phase transmit data bit, the complex programmable logic device being operable to transmit the first in-phase transmit data bit over a first transmission medium in the first set of parallel transmission mediums, the second in-phase transmit data bit over a second transmission medium in the first set of parallel transmission mediums, the first quadrature phase transmit data bit over a third transmission medium in the first set of parallel transmission mediums and the second quadrature phase transmit data bit over a fourth transmission medium in the first set of parallel transmission mediums.

43. The interface of claim 42, wherein the various uplink low rate static/control signals comprises of clock/reference signals, uplink RS-485 based bus data, physical address information, adjacent CDMA channel unit availability information, input information via

uplink serial ports and a radio RF emergency switch, the complex programmable logic device being operable to multiplex the clock/reference signals, adjacent CDMA channel unit availability information, input information via uplink serial ports and a radio RF emergency switch to produce an uplink multiplexed data stream, the complex programmable logic device being operable to transmit the uplink multiplexed data stream over a fifth transmission medium in the first set of parallel transmission mediums, the uplink RS-485 based bus data over a sixth and seventh transmission medium in the first set of parallel transmission mediums and the physical address information over a eighth transmission medium in the first set of parallel transmission mediums.